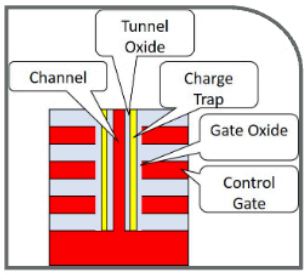
John R. Szedon

Dr. John R. Szedon is the recipient of the 2020 Flash Memory Summit Lifetime Achievement Award for proposing the use of a Charge Trap as a cost-effective memory device.

Dr. John R. Szedon and co-inventor Ting L. Chu (deceased) first presented the concept of using a Charge Trap as a cost-effective memory device in June 1967 at the IEEE Device Research Conference in their paper *Tunnel Inspection and Trapping of Electrons in Aluminum-Silicon Nitride-Silicon Dioxide-Silicon (MNOS) Capacitors*.

Coincidentally, this paper was given in the same year that 2014 FMS Lifetime Achievement Award recipient Dr. Simon Sze co-authored a Bell System Technical Journal paper describing the floating gate while working at Bell Labs. The floating gate has been flash memory's foundational technology since Intel's NOR flash was first shipped in 1987, and flash based on the Charge Trap technique was not productized until 2002. However, as Charge Trap-based 3D NAND has come to dominate flash in recent years, Szedon's proposal has led to the Charge Trap becoming the basis of the great majority of flash chips sold today. As a result, significantly more Charge Trap bits than floating gate cells have shipped over the history of flash memory.



Charge trapping involves electrons that are trapped within the insulating layer between the control gate and the channel of a MOSFET. At the time of the Szedon/Chu paper, Charge Traps were only known as a root cause of the aging that led to field effect transistor failures. Their paper showed that the phenomenon, if properly controlled, could be used to store ones and zeros within a transistor as a memory bit, perhaps replacing that era's magnetic-core memory technology in which hand-woven arrays of magnetic rings were used to store bits. Core memory was very labor-intensive to produce and hence quite costly, and core memory was supplanted by today's popular RAM semiconductor memory starting in the 1970s.

Charge Traps were first commercialized in the early 1970s as a memory device in the MONOS memory element, commonly used in CMOS logic, as well as in SONOS memory chips. This technique was also later used by Advanced Micro Devices, Fujitsu, and Saifun for the MirrorBit 2-bit memory.

Dr. Szedon worked for his entire career at Westinghouse Electric's Science & Technology Center in Churchill, PA, near Pittsburgh, and he co-wrote the 1967 paper as a Senior Research Engineer. His job included identification of certain types of radiation damage in semiconductor devices, and this led to his devising ways to improve their reliability in space vehicles and satellites.

Szedon also performed extensive research in cadmium sulfide solar cells, and he was a very active IEEE volunteer. He edited the IEEE Electron Devices Society's newsletter for a number of years, published over 20 IEEE papers and conference presentations, and was granted four patents. He received all of his degrees from Carnegie Mellon University's College of Engineering: Bachelors in 1959, Masters in 1960, and PhD in 1963.